

Notice of Allowability

Application No.

10/680,170

Examiner

Thanh D. Vo

Applicant(s)

TENG, TOM

Art Unit

2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the Amendment filed on April 18, 2006 and the phone interview on May 24, 2006.
2. ☒ The allowed claim(s) is/are 1-53.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☐ Notice of Informal Patent Application (PTO-152) |
| 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. ☒ Interview Summary (PTO-413),
Paper No./Mail Date ____. |
| 3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date ____ | 7. ☒ Examiner's Amendment/Comment |
| 4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. ☐ Examiner's Statement of Reasons for Allowance |
| | 9. ☐ Other ____. |

DETAILED ACTION

1. This Office Action is responsive to the Amendment filed on April 18, 2006. Claims 7, 17, 32, and 42 are currently amended by Examiner. Claims 1-53 are now in the condition for allowance after Examiner's Amendment.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Gianni Minutoli (Reg. No. 41,198) on May 24, 2006.

3. The application has been amended as follows:

Claim 1. (Previously Presented) A circuit for coordinating refresh and parity-scan operations in a memory device, said circuit comprising:

a plurality of register fields, said register fields containing at least configuration information regarding the memory device; and

control logic coupled to the register fields, said control logic using the information in the register fields to determine whether parity-scan operations can be substituted for refresh operations and scheduling the parity-scan operations instead of refresh

operations when it is determined that the parity-scan operations can be substituted for refresh operations.

Claim 2. (Previously Presented) The circuit of claim 1, wherein said control logic schedules refresh operations if it is determined that parity-scan operations cannot be substituted for refresh operations.

Claim 3. (Previously Presented) The circuit of claim 1, wherein said plurality of register fields comprise configuration register fields containing configuration information.

Claim 4. (Previously Presented) The circuit of claim 3, wherein said plurality of register fields further comprise command register fields containing command information.

Claim 5. (Previously Presented) The circuit of claim 4, wherein said plurality of register fields further comprise status register fields containing status information.

Claim 6. (Previously Presented) The circuit of claim 1, wherein said plurality of register fields comprise:

- configuration register fields containing configuration information;
- command register fields containing command information; and
- status register fields containing status information.

Claim 7. (Currently Amended) The circuit of claim 1, wherein said control logic comprises:

a comparator coupled to said registers fields, said comparator comparing a maximum refresh interval with a maximum parity-scan interval, said comparator outputting a smallest value of said intervals;

counting logic that tracks a next row to be refreshed or parity scanned based at least on the smallest value and a total number of rows to be scanned;

self-refresh logic coupled to the counting logic and being enabled or disabled by information within said registers fields;

parity-scan logic coupled to the counting logic and being enabled or disabled by information within said registers fields; and

coordinating logic for using the information within the registers fields to control the self-refresh logic and the parity-scan logic.

Claim 8. (Previously Presented) The circuit of claim 7, wherein said coordinating logic checks a command stream for idle cycles to insert parity-scan or refresh commands into.

Claim 9. (Previously Presented) The circuit of claim 7 further comprising a multiplexer for selecting an output from said self-refresh logic and said parity-scan logic based on a signal from said coordinating logic.

Claim 10. (Previously Presented) The circuit of claim 7 further comprising:

- a starting scan address register field for storing row address information; and
- a scan completed register field for indicating that all rows have been scanned before the end of a scan period.

Claim 11. (Previously Presented) A memory device comprising:

- a plurality of memory cells organized as an array of rows and columns;
- a plurality of register fields, said register fields containing information regarding the memory device; and
- control logic coupled to the register fields for coordinating refresh and parity-scan operations on the memory cells, said control logic using the information in the register fields to schedule parity-scan operations instead of refresh operations when it is determined that the parity-scan operations can be substituted for refresh operations.

Claim 12. (Previously Presented) The memory device of claim 11, wherein said control logic schedules refresh operations if it is determined that parity-scan operations cannot be substituted for refresh operations.

Claim 13. (Previously Presented) The memory device of claim 11, wherein said plurality of register fields comprise configuration register fields containing configuration information.

Claim 14. (Previously Presented) The memory device of claim 11, wherein said plurality of register fields comprise command register fields containing command information.

Claim 15. (Previously Presented) The memory device of claim 11, wherein said plurality of register fields comprise status register fields containing status information.

Claim 16. (Previously Presented) The memory device of claim 11, wherein said plurality of register fields comprise:

- configuration register fields containing configuration information;
- command register fields containing command information; and
- status register fields containing status information.

Claim 17. (Currently Amended) The memory device of claim 11, wherein said control logic comprises:

- a comparator coupled to said registers fields, said comparator comparing a maximum refresh interval with a maximum parity-scan interval, said comparator outputting a smallest value of said intervals;

- counting logic that tracks a next row to be refreshed or parity scanned based at least on the smallest value and a total number of rows to be scanned;

- self-refresh logic coupled to the counting logic and being enabled or disabled by information within said registers fields;

parity-scan logic coupled to the counting logic and being enabled or disabled by information within said registers fields; and

coordinating logic for using the information within the registers fields to control the self-refresh logic and the parity-scan logic.

Claim 18. (Previously Presented)The memory device of claim 17, wherein said coordinating logic checks a command stream for idle cycles to insert parity-scan or refresh commands into.

Claim 19. (Previously Presented) The memory device of claim 17 further comprising a multiplexer for selecting an output from said self-refresh logic and said parity-scan logic based on a signal from said coordinating logic.

Claim 20. (Previously Presented)The memory device of claim 11 further comprising:
a starting scan address register field for storing row address information; and
a scan completed register field for indicating that all rows have been scanned before the end of a scan period.

Claim 21. (Previously Presented)The memory device of claim 11, wherein said memory cells are dynamic random access memory cells.

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Claim 22. (Previously Presented) The memory device of claim 11, wherein said memory cells are content addressable memory cells comprised of dynamic random access memory.

Claim 23. (Previously Presented) A memory device comprising:

a plurality of register fields, said register fields containing information regarding the memory device; and

means for scheduling parity-scan operations on memory cells of the memory device instead of refresh operations.

Claim 24. (Previously Presented) The memory device of claim 23 further comprising an array of dynamic random access memory cells.

Claim 25. (Previously Presented) The memory device of claim 23 further comprising an array of content addressable memory cells comprised of dynamic random access memory.

Claim 26. (Previously Presented) A processor system comprising:

a processor; and

a memory device coupled to said processor, said memory device comprising a circuit for coordinating refresh and parity-scan operations in said memory device, said circuit comprising:

a plurality of register fields, said register fields containing at least configuration information regarding the memory device; and

control logic coupled to the register fields, said control logic using the information in the register fields to determine whether parity-scan operations can be substituted for refresh operations and scheduling the parity-scan operations instead of refresh operations when it is determined that the parity-scan operations can be substituted for refresh operations.

Claim 27. (Previously Presented) The system of claim 26, wherein said control logic schedules refresh operations if it is determined that parity-scan operations cannot be substituted for refresh operations.

Claim 28. (Previously Presented) The system of claim 26, wherein said plurality of register fields comprise configuration register fields containing configuration information.

Claim 29. (Previously Presented) The system of claim 26, wherein said plurality of register fields further comprise command register fields containing command information.

Claim 30. (Previously Presented) The system of claim 26, wherein said plurality of register fields further comprise status register fields containing status information.

Claim 31. (Previously Presented) The system of claim 26, wherein said plurality of register fields comprise:

- configuration register fields containing configuration information;
- command register fields containing command information; and
- status register fields containing status information.

Claim 32. (Currently Amended) The system of claim 26, wherein said control logic comprises:

- a comparator coupled to said registers fields, said comparator comparing a maximum refresh interval with a maximum parity-scan interval, said comparator outputting a smallest value of said intervals;

- counting logic that tracks a next row to be refreshed or parity scanned based at least on the smallest value and a total number of rows to be scanned;

- self-refresh logic coupled to the counting logic and being enabled or disabled by information within said registers fields;

- parity-scan logic coupled to the counting logic and being enabled or disabled by information within said registers fields; and

- coordinating logic for using the information within the registers fields to control the self-refresh logic and the parity-scan logic.

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Claim 33. (Previously Presented) The system of claim 32, wherein said coordinating logic checks a command stream for idle cycles to insert parity-scan or refresh commands into.

Claim 34. (Previously Presented) The system of claim 32 further comprising a multiplexer for selecting an output from said self-refresh logic and said parity-scan logic based on a signal from said coordinating logic.

Claim 35. (Previously Presented) The system of claim 32 further comprising:

- a starting scan address register field for storing row address information; and

- a scan completed register field for indicating that all rows have been scanned before the end of a scan period.

Claim 36. (Previously Presented) A processor system comprising:

- a processor; and

- a memory device connected to the processor, said memory device comprising:

 - a plurality of memory cells organized as an array of rows and columns;

 - a plurality of register fields, said register fields containing information regarding the memory device; and

 - control logic coupled to the register fields for coordinating refresh and parity-scan operations on the memory cells, said control logic using the information in the register

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fields to schedule parity-scan operations instead of refresh operations when it is determined that the parity-scan operations can be substituted for refresh operations.

Claim 37. (Previously Presented) The system of claim 36, wherein said control logic schedules refresh operations if it is determined that parity-scan operations cannot be substituted for refresh operations.

Claim 38. (Previously Presented) The system of claim 36, wherein said plurality of register fields comprise configuration register fields containing configuration information.

Claim 39. (Previously Presented) The system of claim 36, wherein said plurality of register fields comprise command register fields containing command information.

Claim 40. (Previously Presented) The system of claim 36, wherein said plurality of register fields comprise status register fields containing status information.

Claim 41. (Previously Presented) The system of claim 36, wherein said plurality of register fields comprise:

- configuration register fields containing configuration information;
- command register fields containing command information; and
- status register fields containing status information.

Claim 42. (Currently Amended) The system of claim 36, wherein said control logic comprises:

a comparator coupled to said registers fields, said comparator comparing a maximum refresh interval with a maximum parity-scan interval, said comparator outputting a smallest value of said intervals;

counting logic that tracks a next row to be refreshed or parity scanned based at least on the smallest value and a total number of rows to be scanned;

self-refresh logic coupled to the counting logic and being enabled or disabled by information within said registers fields;

parity-scan logic coupled to the counting logic and being enabled or disabled by information within said registers fields; and

coordinating logic for using the information within the registers fields to control the self-refresh logic and the parity-scan logic.

Claim 43. (Previously Presented) The system of claim 42, wherein said coordinating logic checks a command stream for idle cycles to insert parity-scan or refresh commands into.

Claim 44. (Previously Presented) The system of claim 42, further comprising a multiplexer for selecting an output from said self-refresh logic and said parity-scan logic based on a signal from said coordinating logic.

Claim 45. (Previously Presented) The system of claim 42, further comprising:

a starting scan address register field for storing row address information; and
a scan completed register field for indicating that all rows have been scanned
before the end of a scan period.

Claim 46. (Previously Presented) The system of claim 36, wherein said memory cells are dynamic random access memory cells.

Claim 47. (Previously Presented) The system of claim 36, wherein said memory cells are content addressable memory cells comprised of dynamic random access memory.

Claim 48. (Previously Presented) A processor system comprising:

a processor; and
a memory device connected to the processor, said memory device comprising:
a plurality of register fields, said register fields containing information regarding
the memory device; and
means for scheduling parity-scan operations on memory cells of the memory
device instead of refresh operations.

Claim 49. (Previously Presented) A router comprising:

a plurality of register fields, said register fields containing information regarding the memory device; and

means for scheduling parity-scan operations on memory cells of the memory device instead of refresh operations.

Claim 50. (Previously Presented) A method of coordinating refresh and parity-scanning in a memory array, comprising:

determining whether parity-scan operations can be substituted for refresh operations; and

scheduling the parity-scan operations instead of refresh operations when it is determined that the parity-scan operations can be substituted for refresh operations.

Claim 51. (Previously Presented) The method of claim 50 further comprising the step of scheduling the refresh operations when it is determined that the parity-scan operations cannot be substituted for refresh operations.

Claim 52. (Previously Presented) The method of claim 50 further comprising the step of checking parities returned from the memory array to ensure data integrity.

Claim 53. (Previously Presented) The method of claim 50, wherein the determining step comprises:

comparing a maximum refresh interval to a maximum parity-scan interval;

selecting a smallest parameter of the maximum refresh interval and the maximum parity-scan interval based on the comparison;

dividing the selected smallest parameter by a number of rows per bank to generate a wrap-around limit;

sending an increment signal to a counter when said wrap-around limit is met;

tracking a next row to be refreshed or parity-scanned with said counter;

generating command, enable and address values to be used as values for a parity;

selecting a value indicative of the operation to be performed; and

checking the command stream for idle cycles to insert parity-scan or refresh.

Reason for Allowance

The following is an examiner's statement of reasons for allowance:

Batson '881 discloses a system wherein parity validating is performed concurrently with the refresh operation (see col. 3, lines 34-41 and Fig. 2a-2b). Therefore, Batson '881 teaches a method of combining the parity-scan and refresh operations together (See col. 2, lines 11-15) as a parity-scan operation. However, Batson '881 failed to teach a method in a system where the parity validation is executed instead of refresh operation once it is determined that the parity validation can be substituted for refresh operations as recited in claims 1, 11, 23, 26, 36, 48, 49, and 50.

Claims 2-6, 12-22, 24-31, 37-47, and 51-53 are directly or indirectly depended from allowable claims 1, 11, 23, 36, and 50 respectively, and are allowable along with those independent claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

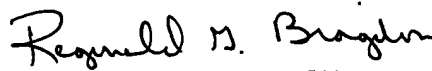
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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5/24/2006



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